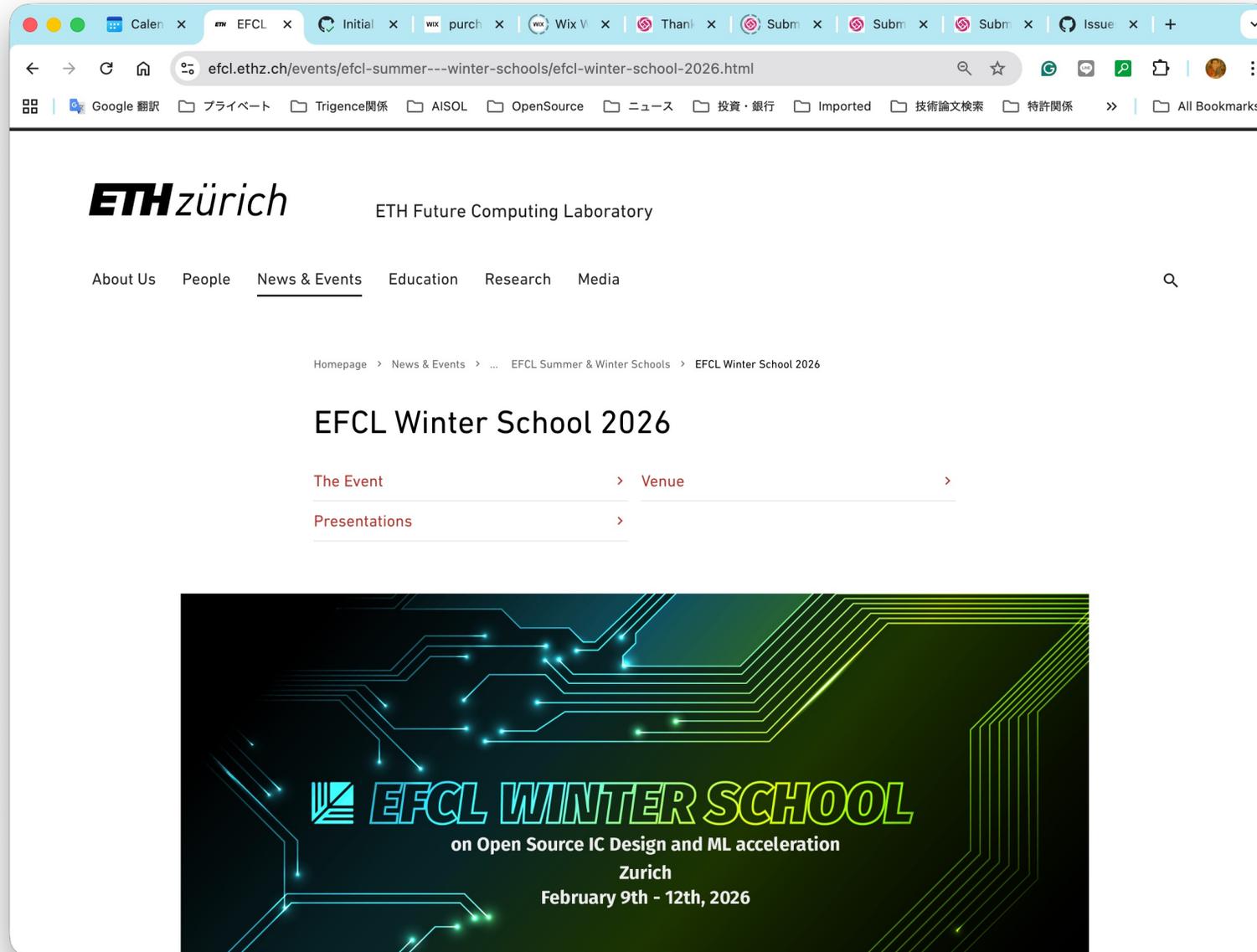




- Open Source Utilized Silicon Initiatives -

AIST Solutions 岡村 淳一

# ETH Zurich Winter School



# ETH Zurich Winter School

The screenshot shows a web browser window displaying the ETH Zurich website. The browser's address bar shows the URL: `efcl.ethz.ch/events/efcl-summer---winter-schools/efcl-winter-school-2026/the-event.html`. The page header features the ETH Zurich logo and the text "ETH Future Computing Laboratory". A navigation menu includes "About Us", "People", "News & Events", "Education", "Research", and "Media". A breadcrumb trail reads: "Homepage > News & Events > EFCL Summer & Winter Schools > EFCL Winter School 2026 > The Event".

## The Event

Keynotes > Track 1 - End-to-end open-source Digital IC Design >

Track 2 - FPGA implementations of RISC-V based micro-controllers with accelerators >

The event will take place from

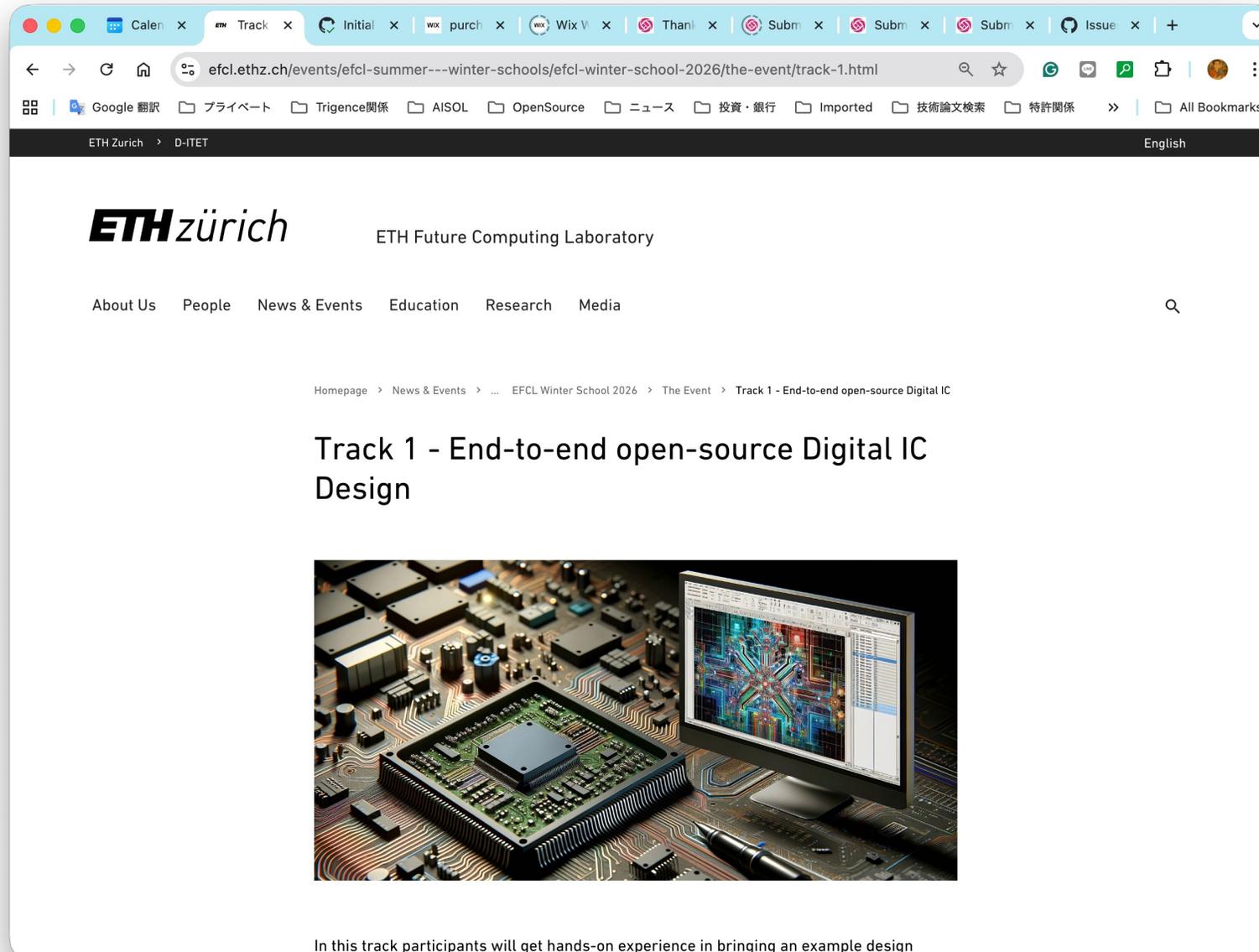
*Monday, February 9th until Thursday, February 12th 2026*

at the ETH Zurich, Electrical Engineering Department at Gloriastrasse 35, 8092 Zurich (working address of Albert Einstein while he was at ETH Zurich) for four days of teaching activities for people that are interested in modern computer architectures, digital IC design, programming of heterogeneous systems and open source hardware.

The event will feature two parallel tracks, running from Tuesday to Thursday. On Monday, the program will begin with a special morning session including lectures and workshops, followed by keynote presentations in the afternoon.

We will round the school with lunches, dinner, and networking apero.

# ETH Zurich Winter School



The screenshot shows a web browser window with the URL `efcl.ethz.ch/events/efcl-summer---winter-schools/efcl-winter-school-2026/the-event/track-1.html`. The page header includes the ETH Zurich logo and the text "ETH Future Computing Laboratory". A navigation menu contains "About Us", "People", "News & Events", "Education", "Research", and "Media". A breadcrumb trail reads: "Homepage > News & Events > ... EFCL Winter School 2026 > The Event > Track 1 - End-to-end open-source Digital IC". The main heading is "Track 1 - End-to-end open-source Digital IC Design". Below the heading is a large image of a computer circuit board with a monitor displaying a circuit design. At the bottom of the page, a paragraph states: "In this track participants will get hands-on experience in bringing an example design".

# ETH Zurich Winter School

activities of the PULP team on open source IC Design.

**Tentative Schedule**

- Day 1 (Tue 10.02.2026):
  - Welcome
  - The case for open source EDA - Frank K. Gürkaynak
  - Exercise: Overview of the design flow
  - Lecture: Front-end design, SystemVerilog refresher
  - Exercise: Simulation
- Day 2 (Wed 11.02.2026):
  - Technical talk - TBD
  - Lecture: Synthesis flow
  - Exercise: Synthesis and understanding timing reports
  - Lecture: Floorplanning, Macro placement, IOs
  - Exercise: Floorplanning
- Day 3 (Thu 12.02.2026):
  - Technical Talk - TBD
  - Lecture: Practical IC design, packaging, testing
  - Exercise: Back-end design flow
  - Exercise: Chip finishing, DRC/LVS
  - Closing

At the end, participants will have experienced a complete digital IC design flow based on open source EDA tools, PDK and designs.

Nine 1.5-hour modules with > 50% hands on exercises in computer laboratory.  
Course will be in English.

Limited to 50 participants

# ETH Zurich Winter School

The screenshot shows a web browser window with the URL `efcl.ethz.ch/events/efcl-summer---winter-schools/efcl-winter-school-2026/presentations.html`. The browser's address bar and tabs are visible at the top. The main content area displays a list of presentations organized into two tracks.

**Onur Mutlu** | [Memory-Centric Computing: Solving Computing's Memory Problem \(PDF, 31.7 MB\) ↓](#)

### Track 1 - End-to-end open-source Digital IC Design

<b>Frank Gurkaynak</b>	<a href="#">Introduction to Open-Source IC Design and PULP (PDF, 10.3 MB) ↓</a>
<b>Phillippe Sauter</b>	<a href="#">Challenges with Basilisk and where the Future is going (PDF, 5.5 MB) ↓</a>
<b>Yichao Zhang, Diyou Shen</b>	<a href="#">Physical Design Is Not Push Button (PDF, 11.8 MB) ↓</a>
<b>Lecture 1</b>	<a href="#">RTL: Refresher on SystemVerilog (PDF, 1.8 MB) ↓</a>
<b>Lecture 2</b>	<a href="#">Netlist: Turning ideas in HDL into physical gates (PDF, 22.9 MB) ↓</a>
<b>Exercise 1</b>	<a href="#">Navigating OpenROAD (PDF, 12.1 MB) ↓</a>
<b>Exercise 2</b>	<a href="#">Simulation with Verilator (PDF, 812 KB) ↓</a>
<b>Exercise 3</b>	<a href="#">Synthesis with Yosys (PDF, 295 KB) ↓</a>
<b>Exercise 4</b>	<a href="#">Floorplanning and Power Grid (PDF, 301 KB) ↓</a>
<b>Exercise 5</b>	<a href="#">Place &amp; Route (PDF, 3.6 MB) ↓</a>
<b>Exercise 6</b>	<a href="#">Finishing and DRC/LVS (PDF, 232 KB) ↓</a>

### Track 2 - FPGA implementations of RISC-V based micro-controllers with accel

<b>Yvan Tortorella</b>	<a href="#">PULP Embedding AI at the Extreme edge of the IoT (PDF, 8.3 MB) ↓</a>
<b>Yvan Tortorella</b>	<a href="#">ISA Extensions in RISC-V-Based Architectures (PDF, 2.9 MB) ↓</a>
<b>Yvan Tortorella</b>	<a href="#">Multicore systems for HPC and edge AI acceleration (PDF, 7.7 MB) ↓</a>
<b>Lecture 1</b>	<a href="#">PULP Platform &amp; PULPissimo architecture (PDF, 3.9 MB) ↓</a>
<b>Lecture 2</b>	<a href="#">Extending RISC-V cores with custom instructions (PDF, 2.6 MB) ↓</a>

[https://ethz.ch/content/dam/ethz/special-interest/itet/efcl-dam/documents/winter-school-2026/track-1/02\\_Phillippe\\_Sauter.pdf](https://ethz.ch/content/dam/ethz/special-interest/itet/efcl-dam/documents/winter-school-2026/track-1/02_Phillippe_Sauter.pdf) nes (HWPEs) (PDF, 3.5 MB) ↓

# ETH Zurich のオープンソースシリコン・設計スクール

ETH Zurich 半導体設計 Winter School に参加してみた！ (1日目)

<https://note.com/jun1okamura/n/nf4313755e040>

ETH Zurich 半導体設計 Winter School に参加してみた！ (2日目)

<https://note.com/jun1okamura/n/n8cf557977df9>

ETH Zurich 半導体設計 Winter School に参加してみた！ (3日目)

<https://note.com/jun1okamura/n/nb7a5f89ac6f7>

ETH Zurich 半導体設計 Winter School に参加してみた！ (4日目)

<https://note.com/jun1okamura/n/na5bb98894143>